COURSE STRUCTURE OF TWO YEAR POST GRADUATE PROGRAM – M.TECH IN EMBEDDED SYSTEMS (EM)

BONAM VENKATA CHALAMAYYA ENGINEERING COLLEGE
ODALAREVU-533210

COURSE STRUCTURE FOR TWO YEAR POST GRADUATE PROGRAM – M.TECH IN EMBEDDED SYSTEMS (EM)

I Semester:

S. No.	Course Code	Subject	L	P	Credits
1	18EM1T01	Digital System Design	3	-	3
2	18EM1T02	Embedded System Design	3	-	3
3	18EM1T03	Embedded Real Time Operating Systems	3	-	3
4	18EM1T04	Embedded – C	3	-	3
5	18EM1D01	**Elective I** 1.Sensors and Actuators	3	-	3
	18EL1D02	2.VLSI Technology & Design			
	18EM1D02	3.Soft Computing Techniques			
	18CO1D09	4.Advanced Computer Architecture			
6	18EM1D03	**Elective II** 1.Embedded Computing	3	-	3
	18EL1D07	2.Network Security & Cryptography			
	18CO1D05	3.Advanced Operating Systems			
	18EM1D04	4.Cyber Security			
7	18EM1L01	Embedded C-Laboratory	--	4	2
Total Credits					**20**

II Semester

S. No.	Course Code	Subject	L	P	Credits
1	18EM2T05	Hardware Software Co-Design	3	-	3
2	18EL2T11	CPLD and FPGA Architectures and Applications	3	-	3
3	18EM2T06	Embedded Networking	3	-	3
4	18EL2T12	Digital Signal Processors and Architecture	3	-	3
5	18EM2D05	**Elective III** 1.CMOS Mixed Signal Circuit Design	3	-	3
	18EM2D06	2.Micro Electro Mechanical System Design			
	18EM2D07	3. Internet Protocols			
	18EM2D08	4. Wireless LANs and PANs			
6	18EM2D09	**Elective IV** 1.System on Chip Design	3	-	3
	18EL2D14	2. Low Power VLSI			
	18EM2D10	3. Multimedia and Signal Coding			
	18EM2D11	4. Asynchronous System Design			
7	18EM2L02	Embedded System Design Laboratory	--	4	2
Total Credits					**20**

III Semester

S. No.	Course Code	Subject	L	P	Credits
1	18EM3V01	Comprehensive Viva-Voce	--	--	2
2	18EM3S01	Seminar – I	--	--	2
3	18EM3P01	Project Work Part – I	--	--	16
Total Credits					**20**

IV Semester

S. No.	Course Code	Subject	L	P	Credits
1	18EM4S02	Seminar – II	--	--	2
2	18EM4P02	Project Work Part - II	--	--	18
Total Credits					**20**

Total No. of Credits – 80

DIGITAL SYSTEM DESIGN

Course Code : 18EM1T01

L	P	C
3	--	3

COURSE OBJECTIVES:

- To understand about the finite state model, capabilities and limitations of FSM and fundamental mode model.
- To understand how to design the digital circuits using ROM's, PLA's and PAL's.
- To understand about the SM charts and their realization and to implement a binary multiplier and a dice game controller.
- To understand about Fault Modeling & Test Pattern Generation and to learn different algorithms for fault diagnosis of Combinational circuits.
- To understand about different methods for fault diagnosis of Sequential circuits.

UNIT-I: Minimization Procedures and CAMP Algorithm:

Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP- I algorithm, Phase-II: Passport checking,Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II: PLA Design, Minimization and Folding Algorithms:

Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT -III: Design of Large Scale Digital Systems:

Algorithmic state machinecharts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV: FAULT DIAGNOSIS IN COMBINATIONAL CIRCUITS:

Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V: FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS:

Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS:

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001, TMH
3. Digital system Design using PLDd-Lala

REFERENCE BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A. Breuer and Arthur D.Friedman- John Wiley & Sons Inc.

COURSE OUTCOMES:

- The students will have the knowledge about the finite state model, capabilities and limitations of FSM and fundamental mode model.
- The students will how to design the digital circuits using ROM's, PLA's and PAL's.
- The students will have the knowledge of SM charts and their realization and to implement a binary multiplier and a dice game controller.
- The students will have the knowledge of Fault Modeling & Test Pattern Generation and different algorithms for fault diagnosis of Combinational circuits.
- The students will understand about different methods for fault diagnosis of Sequential circuits.

EMBEDDED SYSTEMS DESIGN

Course Code: 18EM1T02	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To introduce the difference between embedded systems and general purpose systems.
- To optimize hardware designs of custom single-purpose processors.
- To compare different approaches in optimizing general-purpose processors.
- To introduce different peripheral interfaces to embedded systems.
- To understand the design tradeoffs made by different models of embedded systems.
- To apply knowledge gained in software-hardware integration in team-based projects.

UNIT -I: INTRODUCTION TO EMBEDDED SYSTEMS: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II: TYPICAL EMBEDDED SYSTEM: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III: EMBEDDED FIRMWARE: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV: RTOS BASED EMBEDDED SYSTEM DESIGN: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V: TASK COMMUNICATION: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.

REFERENCE BOOKS:

1. Embedded Systems - Raj Kamal, TMH.
2. Introduction to Embedded Systems - Shibu K.V, McGraw Hill.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

COURSE OUTCOMES:

- Able to Understand the basics of an embedded system
- Able to write Program in embedded system
- Able to Design, implement and test an embedded system.
- Able to introduce different peripheral interfaces to embedded systems.
- Able to understand the design tradeoffs made by different models of embedded systems.
- Able to apply knowledge gained in software-hardware integration in team-based projects.

EMBEDDED REAL TIME OPERATING SYSTEMS

Course Code: 18EM1T03	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To emphasize on the concept of a complete system consisting of asynchronous interactions between concurrently executing hardware components and device driver software in order to illustrate the behavior of a computer system as a whole.
- To understand and design RT Linux and Embedded Linux

UNIT – I: INTRODUCTION: Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II: REAL TIME OPERATING SYSTEMS:

Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III: OBJECTS, SERVICES AND I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV: EXCEPTIONS, INTERRUPTS AND TIMERS: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V: CASE STUDIES OF RTOS: RT Linux, Micro C/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:

1.Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCE BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.

2. Advanced UNIX Programming, Richard Stevens 3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

COURSE OUTCOMES:

- Understand the advanced concepts of computer architecture. Exposing the major differentials of RISC and CISC architectural characteristics.
- Able to investigate modern design structures of Pipelined and Multiprocessors systems
- Able to become acquainted with recent computer architectures and I/O devices, as well as the low-level language required to drive/manage these types of advanced hardware.

EMBEDDED C

Course Code: 18EM1T04 **L p C**

3 --- 3

COURSE OBJECTIVES:

- Understand the significance of programming embedded C in real time applications and to use it for specific applications.
- To gain knowledge on 8051 micro controller
- To develop code for real time embedded world
- To understand design of real time timers with various constraints
- To understand and gain knowledge on Intruder Alarm System.

UNIT – I: PROGRAMMING EMBEDDED SYSTEMS IN C : Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions INTRODUCING THE 8051 MICROCONTROLLER FAMILY: Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements , Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT – II: READING SWITCHES:

Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs(basic code), Example: Counting goats, Conclusions

UNIT – III: ADDING STRUCTURE TO THE CODE: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV: MEETING REAL-TIME CONSTRAINTS: Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V: CASE STUDY: INTRUDER ALARM SYSTEM: Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008

REFERENCE BOOKS:

1. PIC micro MCU C-An introduction to programming, The Microchip PIC in CCS C - Nigel Gardner

COURSE OUTCOMES:

- Able to understand the importance embedded C in so many applications like application specific micro controllers
- Able to develop the quality based embedded systems like Intruder Alarm System
- Able to understand the basic working modes of timers and its formatted data frames, its control.

SENSORS AND ACTUATORS

(ELECTIVE –I)

Course Code: 18EM1D01	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To learn about sensor Principles, Classification, Parameters, Characteristics, Environmental Parameters (EP), and Characterization.
- To know about different sensors like Thermal sensors, Magnetic sensors.
- To know about Smart Sensors, Introduction, Primary Sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication, Standards for Smart Sensor Interface and the Automation

UNIT -I: SENSORS / TRANSDUCERS: Principles – Classification – Parameters – Characteristics – Environmental Parameters (EP) – Characterization. Mechanical and electromechanical sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –TypesCapacitive Sensors: – Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors

UNIT –II: THERMAL SENSORS: Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermo sensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermo emf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors –Anisotropic Magneto resistive Sensing – Semiconductor Magneto resistors– Hall Effect and Sensors –Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros –Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flow meter – Switching Magnetic Sensors SQUID Sensors

UNIT -III: RADIATION SENSORS: Introduction – Basic Characteristics – Types of Photo sensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors. Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential – Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials

– Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media .

UNIT -IV: SMART SENSORS: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation Sensors –applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors –– Sensors for Manufacturing –Sensors for environmental Monitoring

UNIT -V: ACTUATORS: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors

TEXT BOOKS:

1. D. Patranabis – "Sensors and Transducers" –PHI Learning Private Limited. 2. W. Bolton – "Mechatronics" –Pearson Education Limited.

REFERENCE BOOKS:

1. Sensors and Actuators – D. Patranabis – 2nd Ed., PHI, 2013.

COURSE OUTCOMES:

- Able to learn about sensor Principles, Classification, Parameters, Characteristics, Environmental Parameters (EP), and Characterization.
- Able to know about different sensors like Thermal sensors, Magnetic sensors.
- Able to know about Smart Sensors, Introduction, Primary Sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication, Standards for Smart Sensor Interface and the Automation

VLSI TECHNOLOGY AND DESIGN
(ELECTIVE -I)

Course Code: 18EL1D02	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To Understand the vlsi technology and design of circuits based on technology like cmos bicmos etc
- To Understand the designing layouts of logic gates
- To understanding the combinational logic networks and its optimization
- To understanding the sequential systems and its optimization
- To get knowledge on floor plan design

UNIT –I: REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II: LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates &Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III: COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV: SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V: FLOOR PLANNING: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.

2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC

COURSE OUTCOMES:

- Student will be in a position that he/she can design vlsi circuits starting from pmos nmos, cmos, and bicmos technology based design
- Gains thorough knowledge on design tools to draw layouts for the transistor structures
- The student will understand the design of logic gates
- The student will understand the design of sequential systems

SOFT COMPUTING TECHNIQUES

(ELECTIVE -I)

Course Code: 18EM1D02	L	P	C
	3	--	3

COURSE OBJECTIVES:

- To learn about the Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.
- To know about Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm.
- To learn about Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification.
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UNIT –I: INTRODUCTION: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II: ARTIFICIAL NEURAL NETWORKS: Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuronmodel, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III: FUZZY LOGIC SYSTEM: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self organizingfuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV: GENETIC ALGORITHM: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control

problems using genetic algorithm, Concept on some other search techniques like Tabu search and Ant-colony search techniques for solving optimization problems.

UNIT –V: APPLICATIONS: GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of NeuralNetwork interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS:

1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999. 2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCE BOOKS:

1. Fuzzy Sets, Uncertainty and Information - Klir G.J. &Folger T.A., Prentice-Hall of India Pvt.Ltd. 1993.

2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.

3. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.

4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.

5. Elements of Artificial Neural Networks - KishanMehrotra, Chelkuri K. Mohan,Sanjay Ranka, Penram International.

6. Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education.

7. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N.Deepa,1/e, TMH, New Delhi.

COURSE OUTCOMES:

- Able to learn about the Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system,Rule-based systems, the AI approach, Knowledge representation - Expert systems.
- Able to know about Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm.

- Able to learn about Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning,Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification.

ADVANCED COMPUTER ARCHITECTURE

(ELECTIVE -I)

Course Code: 18C01D09 **L p C**

3 --- 3

COURSE OBJECTIVES:

- To emphasize on the concept of a complete system consisting of asynchronous interactions between concurrently executing hardware components and device driver software in order to illustrate the behavior of a computer system as a whole.
- To understand the advanced concepts of computer architecture and exposing the major differentials of RISC and CISC architectural characteristics.

UNIT -I: FUNDAMENTALS OF COMPUTER DESIGN: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

UNIT –II: PIPELINES: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic fivestage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT -III: INSTRUCTION LEVEL PARALLELISM(ILP)-THE HARDWARE APPROACH: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation. ILP Software Approach: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelismat compile time, Cross cutting issues - Hardware verses Software.

UNIT –IV: MULTI PROCESSORS AND THREAD LEVEL PARALLELISM: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V: INTER CONNECTION AND NETWORKS: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

COURSE OUTCOMES:

- Able to understand the advanced concepts of computer architecture and exposing the major differentials of RISC and CISC architectural characteristics.
- Able to investigating modern design structures of Pipelined and Multiprocessors systems.
- Able to become acquainted with recent computer architectures and I/O devices, as well as the low-level language required to drive/manage these types of advanced hardware**.**

EMBEDDED COMPUTING

(ELECTIVE – II)

Course Code: 18EM1D03	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To learn about System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System and Busy Box
- To know about Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls and network security.
- To learn about IA32 Instruction Set, application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools

UNIT –I: PROGRAMMING ON LINUX PLATFORM: System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. Operating System Overview: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

UNIT –II: INTRODUCTION TO SOFTWARE DEVELOPMENT TOOLS:GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools,.

UNIT –III: INTERFACING MODULES: Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, Open CV for machine vision, Audio signal processing.

UNIT –IV: NETWORKING BASICS: Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT –V: IA32 INSTRUCTION SET: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:

1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.

2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS:

1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens

COURSE OUTCOMES:

- Able to learn about System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System and Busy Box
- Able to know about Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls and network security.
- Able to learn about IA32 Instruction Set, application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools

NETWORK SECURITY AND CRYPTOGRAPHY

(ELECTIVE– II)

Course Code: 18EL1D07	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To know about Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security
- To know about Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.
- To know about IP Security Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management

UNIT –I: INTRODUCTION: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT –II: MODERN TECHNIQUES: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations. Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers. Conventional encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation. Public key cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT –III: NUMBER THEORY: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler'stheorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms. Message authentication and hash functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT –IV: HASH AND MAC ALGORITHMS: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. Digital signatures and authentication protocols: Digital signatures, Authentication Protocols, Digital signature standards. Authentication applications: Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT –V: IP SECURITY: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management. Web security: Web Security requirements, Secure sockets layer and Transport layer security,Secure Electronic Transaction. Intruders, viruses and worms: Intruders, Viruses and Related threats. Fire walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.

REFERENCE BOOKS:

1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
2. Network Security - Private Communication in a Public World by Charlie Kaufman, Radia Perlman and Mike Speciner, Pearson/PHI.
3. Principles of Information Security, Whitman, Thomson.
4. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH
5. Introduction to Cryptography, Buchmann, Springer.

COURSE OUTCOMES:

- Able to know about Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security
- Able to know about Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.
- Able to know about IP Security Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management

ADVANCED OPERATING SYSTEMS

(ELECTIVE -II)

Course Code: 18CO1D05	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To learn about Overview of computer system hardware, Instruction execution, I/O function, Interrupts Memory hierarchy, I/O Communication techniques, Operating system objectives and functions.
- To learn about System calls and related file structures, Input / Output, Process creation & termination.
- To learn about Goals of distributed system, Hardware and software concepts and design issues.

UNIT –I: INTRODUCTION TO OPERATING SYSTEMS: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II: INTRODUCTION TO UNIX AND LINUX: Basic commands & command arguments, Standard input, output, Input / output redirection, filter sand editors, Shells and operations

UNIT –III: SYSTEM CALLS: System calls and related file structures, Input / Output, Process creation & termination. Inter process communication: Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams &Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV: INTRODUCTION TO DISTRIBUTED SYSTEMS: Goals of distributed system, Hardware and software concepts, Design issues. Communication in distributed systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V: SYNCHRONIZATION IN DISTRIBUTED SYSTEMS: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:

1. The design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.

3. The Complete reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS:

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems, Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed.John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

COURSE OUTCOMES:

- Able to learn about Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions.
- Able to learn about System calls and related file structures, Input / Output, Process creation & termination.
- Able to learn about Goals of distributed system, Hardware and software

CYBER SECURITY

(ELECTIVE -II)

Course Code: 18EM1D04	**L**	**p**	**C**
	3	**---**	**3**

UNIT I:

Introduction: Security Attacks (Interruption, Interception, Modification and Fabrication), Security Services (Confidentiality, Authentication, Integrity, Non-

repudiation, access Control and Availability) and Mechanisms, A model for Internetwork security, Internet Standards and RFCs, Buffer overflow & format string vulnerabilities, TCP session hijacking, ARP attacks, route table modification, UDP hijacking, and man-in-the-middle attacks.

UNIT II :

Conventional Encryption: Conventional Encryption Principles, Conventional encryption algorithms, cipher block modes of operation, location of encryption devices, key distribution Approaches of Message Authentication, Secure Hash Functions and HMAC

UNIT III : Number Theory: Prime and Relatively Prime Numbers, Modular Arithmetic, Fermat's and Euler's Theorems, The Chinese Remainder theorem, Discrete logarithms Public key: Public key cryptography principles, public key cryptography algorithms, digital signatures, digital Certificates, Certificate Authority and key management Kerberos, X.509 Directory Authentication Service

UNIT IV : IP Security: IP Security Overview, IP Security Architecture, Authentication Header, Encapsulating Security Payload, Combining Security Associations and Key Management Transport Level Security: Web Security Requirements, Secure Socket Layer (SSL) and Transport Layer Security (TLS), Secure Electronic Transaction (SET) Email Privacy: Pretty Good Privacy (PGP) and S/MIME.

UNIT V: Intrusion Detection: Intruders, Intrusion Detection systems, Password Management. Malicious Software: Viruses and related threats & Countermeasures. Fire walls: Firewall Design principles, Trusted Systems.

TEXT BOOKS:

1. Network Security & Cryptography: Principles and Practices, William Stallings, PEA, Sixth edition.

2. Hack Proofing your Network, Russell, Kaminsky, Forest Puppy, Wiley Dreamtech

REFERENCE BOOKS:

1. Network Security & Cryptography, Bernard Menezes, Cengage,2010

EMBEDDED C LABORATORY

Course Code: 18EM1L01	**L**	**p**	**C**
	---	**4**	**2**

NOTE: Minimum of 10 experiments have to be conducted. The following programs have to be tested on 89C51 Development board/equivalent using Embedded C Language on Keil IDE or Equivalent.

1. Program to toggle all the bits of Port P1 continuously with 250 mS delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
10. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions
11. Program to Sort RTOS on to 89C51 development board. 12. Program to interface Elevator.

Semester-II

HARDWARE SOFTWARE CO-DESIGN

Course Code: 18EM2T05	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To design mixed hardware-software systems and the design of hardware-software interfaces
- To focus on common underlying modeling concepts, and the trade-offs between hardware and software components.
- To learn about System –level specification, design representation for system level synthesis, system level specification languages.
-

UNIT –I: CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- synthesis algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co synthesis.

UNIT –II: PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure Target architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III: COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV: DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V: LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages, Languages for system – level

specification and design-ii: Heterogeneous specifications and multi language cosimulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010Springer

COURSE OUTCOMES:

- Able to design mixed hardware-software systems and the design of hardware-software interfaces
- Able to focus on common underlying modeling concepts, , and the trade-offs between hardware and software components.
- Able to learn about System –level specification, design representation for system level synthesis, system level specification languages**.**

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

Course Code: 18EL2T11	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To understand the types of programmable logic devices and what are the differences between these devices. What are the different complex programmable logic devices with examples.
- To know the types of FPGA's and their programming technologies. What are the programmable logic block architectures, their interconnects and what are applications of FPGA's.
- To understand about the SRAM programmable FPGA's and their programming technology. What are examples of SRAM programmable FPGA's i.e Xilinx FPGA's with block diagrams.

UNIT-I: INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation**.**

UNIT-II: FIELD PROGRAMMABLE GATE ARRAYS: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III: SRAM PROGRAMMABLE FPGAS: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 andXC4000 Architectures.

UNIT -IV: ANTI-FUSE PROGRAMMED FPGAS: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3Architectures.

UNIT -V: DESIGN APPLICATIONS: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.

2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.

2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.

3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.

4. FPGA based System Design -Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

COURSE OUTCOMES:

- The students will have the knowledge of types of programmable logic devices and what are the differences between these devices.
- The students will have the knowledge of types of FPGA's and their programming technologies, programmable logic block architectures, their interconnects and what are applications of FPGA's.
- The students will be able to know the programming technology of SRAM programmable FPGA's with their internal logic diagrams.

EMBEDDED NETWORKING

Course Code: 18EM2T06	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To understand the significance of embedded networks in real time applications and to use it for specific applications.
- To Know different types of communication protocols like serial and parallel communication protocols

- To know different types of communication protocols which have embedded end modules
- To understand wired and wireless communication protocols, its formats
- To understand and gain knowledge on wireless sensors and its application in wireless embedded networks

UNIT –I: Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols - RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols –Firewire.

UNIT –II: USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing –PIC microcontroller CAN Interface –A simple application with CAN.

UNIT –III: Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

UNIT –IV: Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT –V: Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing –Data Centric routing.

TEXT BOOKS:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, TonyGivargis, John & Wiley Publications, 2002

2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port -Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series -Dogan Ibrahim, Elsevier 2008.

2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.

3. Networking Wireless Sensors – Bhaskar Krishnamachari, Cambridge press 2005.

COURSE OUTCOMES:

- Able to understand the basic working modes of networks and its formatted data frames, its control
- Able to understand the significance of embedded networks in real time applications and to use it for specific applications.
- Able to Know different types of communication protocols like serial and parallel communication protocols
- Able to know different types of communication protocols which have embedded end modules
- Able to understand wired and wireless communication protocols, its formats
- Able to understand and gain knowledge on wireless sensors and its application in wireless embedded network.

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

Course Code: 18EL2T12	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- Gives an over view of entire digital signal processing techniques i.e. convolution, DFT, FFT, IIR & FIR filters. The fixed and floating point representation, different types of errors introduced during A-D and D-A converter stage
- To introduce the DSP computational building blocks and special types of addressing modes compared to normal microprocessor

- To introduce architectural features of programmable DSP Processors of TMS320C54XX processor. To develop the programming knowledge using Instruction set of DSP Processors
- To introduce architectural features of analog devices family of DSP devices i.e. ADSP 2100, ADSP 2181 and blackfin processor
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UNIT –I: INTRODUCTION TO DIGITAL SIGNAL PROCESSING: Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation. Computational accuracy in dsp implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II: ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing**.**

UNIT -III: PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XXProcessors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV: ANALOG DEVICES FAMILY OF DSP DEVICES: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals

UNIT –V: INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.

2. A Practical Approach to Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, , New Age International, 2006/2009

3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M.Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani andM. Bhaskar, 2002, TMH.

2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.

3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.

4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI

5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997

6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes ,ISBN 0750679123, 2005

COURSE OUTCOMES:

- Able to gives an over view of entire digital signal processing techniques i.e. convolution, DFT, FFT, IIR & FIR filters. The fixed and floating point representation, different types of errors introduced during A-D and D-A converter stage
- Able to introduce the DSP computational building blocks and special types of addressing modes compared to normal microprocessor

- Able to introduce architectural features of programmable DSP Processors of TMS320C54XX processor. To develop the programming knowledge using Instruction set of DSP Processors
- Able to introduce architectural features of analog devices family of DSP devices i.e. ADSP 2100, ADSP 2181 and blackpin processor.

CMOS MIXED SIGNAL CIRCUIT DESIGN
(ELECTIVE III)

Course Code: 18EM2D05	**L**	**p**	**C**
	3	**---**	**3**

UNIT-I:

Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Nonideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-II:

Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge

pump PLL, Non-ideal effects in PLLsPFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III:

Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV:

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT-V:

Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibitquantizers, Delta sigma D/A

TEXT BOOKS:

. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002

2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. . Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003

2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.

3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

MICRO ELECTRO MECHANICAL SYSTEM DESIGN (ELECTIVE III)

Course Code: 18EM2D06	**L**	**p**	**C**
	3	**---**	**3**

Course Objectives

- To learn basics of Micro Electro Mechanical Systems (MEMS).
- To learn about various sensors and actuators used in MEMS.
- To learn the principle and various devices of MOEMS, Fluidic, bio and chemical systems.

UNIT-I:

Introduction Basic structures of MEM devices – (Canti-Levers, Fixed Beams diaphragms).Broad Response of Micro electromechanical systems (MEMS) to Mechanical

(Force, pressure etc.)Thermal, Electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc.

UNIT-II:

Review Review of mechanical concepts like stress, strain, bending moment, deflection curve. Differential equations describing the deflection under concentrated force, Distributed force, distributed force, Deflection curves for canti-levers- fixed beam. Electrostatic excitation – columbic force between the fixed and moving electrodes.Deflection with voltage in C.L, Deflection Vs Voltage curve, critical fringe field – field calculations using Laplace equation.Discussion on the approximate solutions – Transient response of the MEMS.

UNIT-III:

Types Two terminal MEMS - capacitance Vs voltage Curve – Variable capacitor.Applications of variable capacitors.Two terminal MEM structures.Three terminal MEM structures – Controlled variable capacitors – MEM as a switch and possible applications.

UNIT-IV:

MEM Circuits & Structures MEM circuits & structures for simple GATES- AND, OR, NAND, NOR, Exclusive OR, simple MEM configurations for flip-flops triggering applications to counters, converters. Applications for analog circuits like frequency converters, wave shaping. RF Switches for modulation. MEM Transducers for pressure, force temperature.Optical MEMS.

UNIT-V:

MEM Technologies Silicon based MEMS- Process flow – Brief account of various processes and layers like fixed layer, moving layers spacers etc., and etching technologies. Metal Based MEMS: Thin and thick film technologies for MEMS. Process flow and description of the processes, Status of MEMS in the current electronics scenario.

TEXT BOOKS:

1. MEMS Theory, Design and Technology - GABRIEL. M.Review, R.F.,2003, John wiley& Sons. .

2. Strength of Materials –ThimoShenko, 2000, CBS publishers & Distributors. 3. MEMS and NEMS, Systems Devices; and Structures - ServeyE.Lyshevski, 2002, CRC Press.

REFERENCE BOOKS:

1. Sensor Technology and Devices - Ristic L. (Ed) , 1994, Artech House, London.

Course outcomes

Upon successful completion of this course the student shall be able to know the importance and various devices of MEMS and their applications.

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INTERNET PROTOCOLS
(ELECTIVE III)

Course Code: 18EM2D07	**L**	**p**	**C**
	3	**---**	**3**

UNIT -I:

Internetworking Concepts: Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level Interconnection, Properties of thee Internet, Internet Architecture, Wired LANS, Wireless LANs, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite. IP Address: Classful Addressing: Introduction, Classful Addressing, Other Issues, Sub-netting and Supernetting Classless Addressing: Variable length Blocks, Sub-netting, Address Allocation. Delivery, Forwarding, and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router. ARP and RARP: ARP, ARP Package, RARP.

UNIT -II:

Internet Protocol (IP): Datagram, Fragmentation, Options, Checksum, IP V.6. Transmission Control Protocol (TCP): TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times. Stream Control Transmission Protocol (SCTP): SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control. Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP. Classical TCP Improvements: Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/ Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP.

UNIT -III:

Unicast Routing Protocols (RIP, OSPF, and BGP): Intra and Inter-domain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP. Multicasting and Multicast Routing Protocols: Unicast - Multicast- Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing: MOSPF, Multicast Distance Vector: DVMRP.

UNIT -IV:

Domain Name System (DNS): Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet. Remote Login TELNET: Concept, Network Virtual Terminal (NVT). File Transfer FTP and TFTP: File Transfer Protocol (FTP). Electronic Mail: SMTP and POP. Network Management-SNMP: Concept, Management Components, World Wide Web- HTTP Architecture.

UNIT -V:

Multimedia: Digitizing Audio and Video, Network security, security in the internet firewalls. Audio and Video Compression, Streaming Stored Audio/Video, Streaming Live Audio/Video, Real-Time Interactive Audio/Video, RTP, RTCP, Voice Over IP. Network Security, Security in the Internet, Firewalls.

TEXT BOOKS:

1. TCP/IP Protocol Suite- Behrouz A. Forouzan, Third Edition, TMH
2. Internetworking with TCP/IP Comer 3 rd edition PHI

REFERENCE BOOKS:

1. High performance TCP/IP Networking- Mahbub Hassan, Raj Jain, PHI, 2005
2. Data Communications & Networking – B.A. Forouzan– 2nd Edition – TMH
3. High Speed Networks and Internets- William Stallings, Pearson Education, 2002.
4. Data and Computer Communications, William Stallings, 7th Edition., PEI.
5. The Internet and Its Protocols – AdrinFarrel, Elsevier, 2005.

WIRELESS LANS AND PANS
(ELECTIVE III)

Course Code: 18EM2D08	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To learn about First and Second Generation Cellular Systems, Cellular Communications from 1G to3G, Wireless 4G systems.
- To know about importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies infrared technology, UHF narrowband technology, Spread Spectrum technology

To learn about Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem and Reliability

UNIT –I: Wireless System & Random Access Protocols: Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to 3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).

UNIT –II: Wireless LANs: Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology

UNIT –III: The IEEE 802.11 Standard for Wireless LANs: Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol

UNIT –IV: Wireless PANs: Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assignment, Scatternet formation.

UNIT –V: The IEEE 802.15 working Group for WPANs: The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband.

TEXT BOOKS:

1. Ad Hoc and Sensor Networks - Carlos de MoraisCordeiro and Dharma PrakashAgrawal, World Scientific, 2011.

2. Wireless Communications and Networking - Vijay K.Garg, Morgan Kaufmann Publishers, 2009.

REFERENCE BOOKS

1. Wireless Networks - KavehPahlaram, Prashant Krishnamurthy, PHI, 2002.

2. Wireless Communication- Marks Ciampor, JeorgeOlenewa, Cengage Learning, 2007.

COURSE OUTCOMES:

- Able to learn about First and Second Generation Cellular Systems, Cellular Communications from 1G to3G, Wireless 4G systems.
- Able to know about importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison

of wired and Wireless LANs; WLAN Technologies infrared technology, UHF narrowband technology, Spread Spectrum technology

- Able to learn about Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem and Reliability.

SYSTEM ON CHIP ARCHITECTURE

(ELECTIVE -IV)

Course Code: 18EM2D09	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- Instruction to system approach deals with how system assembled with the components, which components are involved in the system integration.
- To introduce hardware and software programmability verses performance
- To know about entire memory organization, starch pads, cache memories and objective in cache data how to deal the write polices
-

UNIT –I: INTRODUCTION TO THE SYSTEM APPROACH: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II: PROCESSORS: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III: MEMORY DESIGN FOR SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV: INTERCONNECT CUSTOMIZATION AND CONFIGURATION: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V: APPLICATION STUDIES / CASE STUDIES: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely IndiaPvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer

2. Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.

3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, PeterPaterson and Leena Singh L, 2001, Kluwer Academic Publishers.

COURSE OUTCOMES:

- Able to about how the system forms with the lot of component and has majority about system level interconnections
- Able to introduce hardware and software programmability verses performance
- Able to know about entire memory organization, starch pads, cache memories and objective in cache data how to deal the write polices

LOW POWER VLSI
(ELECTIVE-IV)

Course Code : 18EL2D14	**L**	**P**	**C**
	3	**--**	**3**

UNIT-I: Fundamentals of Low Power VLSI Design Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT-II: Low-Power Design Approaches Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach – Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT-III: Low-Voltage Low-Power Adders Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT-IV: Low-Voltage Low-Power Multipliers Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT-V: Low-Voltage Low-Power Memories Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
2. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000. 3. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
4. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

MULTI MEDIA AND SIGNAL CODING

(ELECTIVE -IV)

Course Code: 18EM2D10	**L**	**p**	**C**
	3	**---**	**3**

COURSE OBJECTIVES:

- To learn about Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.
- To know about Lossless compression algorithms like Run Length Coding, Variable Length Coding, Arithmetic Coding and Lossless JPEG image Compression.
- To learn about Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT -I: INTRODUCTION TO MULTIMEDIA: Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats. COLOR IN IMAGE AND VIDEO: Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Out of-Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model.

UNIT -II: VIDEO CONCEPTS: Types of Video Signals, Analog Video, Digital Video. AUDIO CONCEPTS: Digitization of Sound, Quantization and Transmission of Audio.

UNIT -III: COMPRESSION ALGORITHMS: Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression. Lossy Image Compression Algorithms: Transform Coding: KLT And DCT Coding, Wavelet Based Coding. Image Compression Standards: JPEG and JPEG2000.

UNIT -IV: VIDEO COMPRESSION TECHNIQUES: Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding,Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT -V: AUDIO COMPRESSION TECHNIQUES: ADPCM in Speech Coding, G.726 ADPCM, Vocoders – Phase Insensitivity, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

TEXT BOOKS:

1. Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI, 2010.

2. Multimedia Signals & Systems – Mrinal Kr. Mandal Springer International Edition 1st Edition, 2009

REFERENCE BOOKS:

1. Multimedia Communication Systems – Techniques, Stds &Netwroks K.R. Rao, Zorans.Bojkoric, DragoradA.Milovanovic, 1st Edition, 2002.

2. Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition,2009.

3. Multimedia Systems John F. KoegelBufond Pearson Education (LPE), 1st Edition, 2003.

4. Digital Video Processing – A. Murat Tekalp, PHI, 1996.

5. Video Processing and Communications – Yaowang, JornOstermann, Ya-QinZhang, Pearson,2002

COURSE OUTCOMES:

- Able to learn about Multimedia, World Wide Web, Overview of Multimedia Tools,Multimedia Authoring, Graphics/ Image Data Types, and File Formats.
- Able to know about Lossless compression algorithms like Run Length Coding, Variable Length Coding, Arithmetic Coding and Lossless JPEG image Compression.
- Able to learn about Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

ASYNCHRONOUS SYSTEM DESIGN

(ELECTIVE -IV)

Course Code: 18EM2D11	**L**	**p**	**C**
	3	**---**	**3**

UNIT-I: FUNDAMENTALS: Handshake protocols, Muller C-element, Muller pipeline, Circuit implementation styles, theory. Static data-flow structures: Pipelines and rings, Building blocks, examples.

UNIT-II: PERFORMANCE: A quantitative view of performance, quantifying performance, Dependency graphic analysis. Handshake circuit implementation: Fork, join, and merge, Functional blocks, mutual exclusion, arbitration and metastability.

UNIT-III: SPEED-INDEPENDENT CONTROL CIRCUITS: Signal Transition graphs, Basic Synthesis Procedure, Implementation using state-holding gates, Summary of the synthesis Process, Design examples using Petrify. Advanced 4-phase bundled data protocols and circuits: Channels and protocols, Static type checking, More advanced latch control circuits.

UNIT-IV: HIGH-LEVEL LANGUAGES AND TOOLS: Concurrency and message passing in CSP, Tangram program examples, Tangram syntax directed compilation, Martin's translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools.

UNIT-V: THE BALSA LANGUAGE: Data types, Control flow and commands, Binary/Unary operators, Program structure. Building library Components: Parameterized descriptions, Recursive definitions. A simple DMA controller: Global Registers, Channel Registers, DMA control structure, The Balsa description.

Principles of Asynchronous Circuit Design - Jens Sparso, Steve Furber, Kluver Academic Publishers.

TEXT Books:

- Asynchronous Circuit Design- Chris. J. Myers, John Wiley & Sons,2001.
- Handshake Circuits An Asynchronous architecture for VLSI programming – Kees Van Berkel Cambridge University Press, 2004
- Principles of Asynchronous Circuit Design-Jens Sparso, Steve Furber, Kluver Academic Publishers, 2001.

EMBEDDED SYSTEM DESIGN LABORATORY

Course Code: 18EM2L02	**L**	**p**	**C**
	---	**4**	**2**

A. The following programs are to be implemented on ARM based Processors/Equivalent.

B. B. Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

PART- I: The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for a. Addition | Subtraction | Multiplication | Division b. Operating Modes, System Calls and Interrupts c. Loops, Branches 2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.

3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.

4. Program for reading and writing of a file

5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment

6. Program to demonstrates a simple interrupt handler and setting up a timer

7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.

8. Program to Interface 8 Bit LED and Switch Interface

9. Program to implement Buzzer Interface on IDE environment

10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.

11. Program to demonstrate I2C Interface on IDE environment

12. Program to demonstrate I2C Interface – Serial EEPROM

13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.

14. Generation of PWM Signal 15. Program to demonstrate SD-MMC Card Interface.

PART- II: Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.

2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task

3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher

priority than external interrupt button)

4. a).Write an application to Test message queues and memory blocks. b).Write an application to Test byte queues

5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings

7. Write an application that creates a two task displaying two different messages in LCD display in two lines.

8. Sending messages to mailbox by one task and reading the message from mailbox by another task.

9. Sending message to PC through serial port by three different tasks on priority Basis.

10. Basic Audio Processing on IDE environment